has been developed which is effective for obtaining a high breakdown voltage in a blocking state (OFF-state) or at the time of turning-off at a junction terminating region portion which is positioned at the outer periphery of an element active region portion (hereinafter referred to as a cell region portion) and which is a region portion for maintaining the breakdown voltage by attenuating the electrical field by extending the depletion layers. Therefore, because the way of spreading of the depletion layers in the cell region portion and the junction terminating region portion are different from one another, the optimum impurity concentrations are different from one another. Accordingly, if the device is manufactured such that the impurity amounts in the cell region portion and the junction terminating region portion are the same, the breakdown voltage at the terminating portion decreases, and an electric field locally concentrates at this place. As a result, there are cases in which the device is broken. In this way, there is the problem that a sufficiently high breakdown voltage cannot be obtained by the entire device in the prior art.

[0014] Further, because there are dispersions among the processes at the time of actual manufacturing, it is difficult to make the respective impurity amounts of the n− type drift layer **102** and the p type drift layer **106** completely equal, and the breakdown voltage deteriorates in accordance therewith. Accordingly, it is necessary to carry out designing of the device in consideration of such a decrease of the breakdown voltage due to the process margin. In order to lower the ON-state resistance, it is effective to raise the impurity concentration of the n− type drift layer **102**. On the other hand, the process margin for the breakdown voltage is determined by the difference in the impurity amounts between the n− type drift layer **102** and the p type drift layer **106**. Therefore, when the impurity amount of the n− type drift layer **102** is increased, because the difference itself determining the process margin is not changed, the ratio between the allowed impurity amount and the impurity amount of the n− type drift layer **102** becomes small. Namely, the process margin becomes small.

BRIEF SUMMARY OF THE INVENTION

[0015] According to a first aspect of the present invention, there is provided a semiconductor device comprising:

[0016] a first-first conductivity type semiconductor layer which includes a cell region portion and a junction terminating region portion, the junction terminating region portion being a region portion which is positioned in an outer periphery of the cell region portion to maintain a breakdown voltage by extending a depletion layer to attenuate an electric field;

[0017] a second-first conductivity type semiconductor layer which is formed on one surface of the first-first conductivity type semiconductor layer;

[0018] a first main electrode which is electrically connected to the second-first conductivity type semiconductor layer;

[0019] first-second conductivity type semiconductor layers which are formed in the cell region portion of the first-first conductivity type semiconductor layer in substantially vertical directions to the one surface of the first-first conductivity type semiconductor layer, respectively, and which are periodically disposed in a first direction which is an arbitrary direction parallel to the one surface;

[0020] a second-second conductivity type semiconductor layer which is selectively formed in the other surface portion of the first-first conductivity type semiconductor layer so as to contact the first-second conductivity type semiconductor layers;

[0021] a third-first conductivity type semiconductor layer which is selectively formed in the surface portion of the second-second conductivity type semiconductor layer;

[0022] a second main electrode which is formed so as to contact the second-second conductivity type semiconductor layer and the third-first conductivity type semiconductor layer;

[0023] a control electrode which is formed on the surface of the first-first conductivity type semiconductor layer sandwiched by the adjacent second-second conductivity type semiconductor layers, the surface of the adjacent second-second conductivity type semiconductor layers and the surface of the third-first conductivity type semiconductor layer, with a gate insulating film interposed therebetween; and

[0024] third-second conductivity type semiconductor layers which are formed in the junction terminating region portion and are periodically disposed in at least one direction of the first direction and a second direction perpendicular to the first direction.

[0025] According to a second aspect of the invention, there is provided a method of manufacturing a semiconductor device having a super junction structure with a first conductivity type semiconductor layer on which a trench groove whose aspect ratio is R is provided and a second conductivity type semiconductor layer which is buried in the trench groove, the method of manufacturing the semiconductor device comprising:

[0026] forming a trench groove having an aspect ratio of R/N (N is a natural number greater than 1) in a first conductivity type semiconductor layer;

[0027] epitaxially growing a second conductivity type semiconductor layer so as to bury the trench groove;

[0028] removing the second conductivity type semiconductor layer until a surface of the first conductivity type semiconductor layer is exposed;

[0029] epitaxially growing the first conductivity type semiconductor layer on the first conductivity type semiconductor layer and the second conductivity type semiconductor layer such that the thickness of the first conductivity type semiconductor layer increases by a length which is substantially the same as a depth of the trench groove formed by the first process;

[0030] selectively removing the first conductivity type semiconductor layer such that the second con-